REMARKS/ARGUMENTS

Claims 1-5, 9, 10, 12-16, 20, and 21 stand rejected under 35 U.S.C. 102(b) as being anticipated by Wendell.

Claim 1 comprises the limitations of an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and

an array low voltage control circuitry that provides an enhanced low operating voltage V_{ESS} to said SRAM array during at least a portion of a READ operation or a WRITE operation thereof, said enhanced low operating voltage V_{ESS} having a higher value than a low operating voltage V_{SS}.

The Wendell reference describes a SRAM cell with a high voltage VDD and a low voltage VSS (col. 4, lines 54-67). The Wendell reference defines a terminal VDDWL to which the "voltage presented to this terminal VDDWL may be tied to the standard VDD voltage used for normal operation of the memory array 10, but may also be tied for test purposes to voltages other than the standard VDD." The voltage that is varied in the Wendell is the VDD voltage and not the low operating voltage Vss. Claim 1 of the instant invention explicitly claims the variation of the Vss voltage which is fixed in the Wendell reference. In fact the Wendell reference does not disclose a mechanism by which the Vss voltage can be varied. Claim 1 of the instant invention is allowable over the cited prior art reference. Claims 5-10 depend on claim 1 and therefore contain all the limitations of claim 1. Claims 5-10 are therefore also allowable over the cited art.

Claim 12 comprises the limitations of employing in an integrated circuit an SRAM array coupled to row peripheral circuitry by a word line and coupled to column peripheral circuitry by bit lines; and providing an enhanced low operating voltage V_{ESS} to said SRAM array during at least a portion of an active mode, said enhanced low operating voltage V_{ESS} having a higher value than a low operating voltage V_{SS}. As described above the Wendell reference does describe nor provide a mechanism to vary the low operating voltage Vss. Claim 12 comprises the limitation of providing an

enhanced low operating voltage having a higher value than Vss. Claim 12 is therefore allowable over the cited prior art reference. Claims 13-21 depends on claim 12 and therefore contain all the limitations of claim 12. Claims 13-21 are therefore allowable over the cited prior art reference.

Applicant appreciates the indication that claims 6-8 and 17-19, if rewritten in independent form including all of the limitations of the base claim and any intervening claims, would be allowable.

In light of the above, it is respectfully submitted that the present application is in condition for allowance, and notice to that effect is respectfully requested.

While it is believed that the instant response places the application in condition for allowance, should the Examiner have any further comments or suggestions, it is respectfully requested that the Examiner contact the undersigned in order to expeditiously resolve any outstanding issues.

To the extent necessary, Applicant petitions for an Extension of Time under 37 CFR 1.136. Please charge any fees in connection with the filing of this paper, including extension of time fees, to the deposit account of Texas Instruments Incorporated, Account No. 20-0668.

Respectfully submitted,

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